REMARKS

Claims 1, 3-14, 16-19, 21-24, and 31-54 remain in this application. No claims have been added, amended, or cancelled. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §103(a) Rejection – Gates in view of Carlsson et al.

The Examiner has rejected claims 1, 4-6, 9-14, 16-19, 21-24 and 31-54 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5, 701, 409 to Gates (hereinafter "Gates") in view of U.S. Patent No. 4,053,947 to Carlsson et al. ("Carlsson").

Claim 1 and Dependent Claims

Claim 1 recites, "*A system comprising an instruction memory to store a plurality of predefined bus stimuli instructions that represent a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases, and one or more phase generators coupled with a bus and the instruction memory, the one or more phase generators to drive a series of signals on the bus corresponding to the predefined sequence of bus transactions*". Gates in view of Carlsson does not teach or suggest a predefined sequence of multiple-phase bus transactions.

Claim 1 is directed to a system to drive a predefined sequence of multiple-phase bus transactions on a bus. As discussed in the application at page 7, components such as processors and chipsets coupled to complex buses often contain bugs that cause them to fail during operation. In the failing scenarios, the components frequently respond incorrectly to specific bus transaction sequences, even when the bus transaction sequence is "legal"; in other words, there is nothing in the bus transaction sequence that should have caused the component to fail. The purpose of correcting these bugs may involve

inducing the failure under controlled conditions to isolate the bug. Accordingly, driving a predefined sequence of multiple-phase bus transactions have uses in isolating and correcting bugs in processors, chipsets, and other components.

Gates does not teach or suggest a predefined sequence of multiple-phase bus transactions. Rather, Gates discusses an entirely different approach for error generation, wherein a bus error generation circuit generates an error on the bus in response to a single error command rather than a predefined sequence of bus transactions. "To test the PCI bus, a device on the PCI bus loads an error command into a command register of the bus error generation circuit of the integrated circuit via the PCI bus" (column 2, lines 39-42). Error generation is caused by a single command instead of a predefined sequence of bus transactions. The single commands are shown in Figure 7. The Examiner is respectfully referred to Figures 9A-9H and the associated text for detailed examples of how the single commands cause error generation by inversion of a parity bit. In short, the single command forces an error through a bus error generation circuit intentionally inverting the parity bit. "Writing of this command causes the incorrect parity control circuit 110 to generate an error on the PCI bus 101" (column 5, lines 10-12). "After a particular error command is loaded into the command register of the bus error generation circuit of the master device, the bus error generation circuit causes an incorrect parity value to be output onto the PCI bus terminal PAR during a subsequent data write PCI bus cycle" (column 2, lines 49-53). The parity bit inversion is done by the incorrect parity control circuits 110 and 209 shown in Figures 3 and 5, respectively. An example of this is explained as follows, "[r]ather than controlling gate 109 to output the correct parity on lead 111, however, incorrect parity control circuit 110 controls gate 109 to output the incorrect parity value onto parity bus terminal 106 in order to simulate an error on the PCI bus 101" (column 4, lines 37-42).

The Applicants have reviewed Gates and have found no teaching or suggestion whatsoever of a sequence of commands let alone using a sequence of commands for error correction. Accordingly, the concepts of a predetermined sequence of bus transactions and of using the predetermined sequence for error detection are completely foreign to Gates. The Examiner appears to admit this when he stated that Gates fails to teach storing more than one command.

The Examiner has also stated that it would have been obvious to one of ordinary level of skill in the art at the time the invention was made to modify Gates to include multiple phase transactions, as taught by Carlsson, to increase processing time and simplify the system. The Applicants respectfully disagree. The prior-art references do not contain any suggestion, either express or implied, that they be combined in the manner suggested. Gates does not suggest that increased processing time or a simplified system would be desirable and accordingly a person having an ordinary level of skill in the art would not be motivated to modify Gates with Carlsson. Additionally, the Applicants respectfully submit that the complete lack of a discussion of error generation makes it unlikely that a person of ordinary skill in the art would find the discussion in Carlsson relevant in any way to using the disclosure therein in combination with the error generation discussed in Gates. Furthermore, there is no indication whatsoever that the modification would in fact increase processing time or simplify the system. Additionally, the references are each individually complete so there would be no reason to substitute parts of Carlsson into Gates. Accordingly, the modification of Gates is believed to be inappropriate and claim 1 is believed to be allowable.

Accordingly, claim 1 is believed to be allowable. Claims 3-14 and 32-33 depend from claim 1 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 16 and Dependent Claims

Claim 16 recites, "*instructions representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases*". Accordingly, claim 16 is believed to be allowable for reasons similar to those discussed above for claim 1. Claims 17-19 depend from claim 16 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 21 and Dependent Claims

Claim 21 recites, "*receiving instruction words representing a predefined sequence of bus transactions, wherein each transaction has multiple transaction phases*". Accordingly, claim 21 is believed to be allowable for reasons similar to those discussed above for claim 1. Claims 22-24 depend from claim 21 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 31

Claim 31 recites, "*generating a plurality of instruction words corresponding to a predefined sequence of bus transactions, wherein each transaction has multiple phases*". Accordingly, claim 31 is believed to be allowable for reasons similar to those discussed above for claim 1.

Claim 34 and Dependent Claims

Claim 34 recites, "*a representation of a predefined sequence of bus stimuli associated with multiple phase bus transactions*". Accordingly, claim 34 is believed to be allowable for reasons similar to those discussed above for claim 1. Claims 35-47 depend from claim 34 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 48 and Dependent Claim

Claim 48 recites, "*debug means coupled with the bus for asserting a legal sequence of multiple phase bus transactions on the bus and for allowing determination of an incorrect response to the sequence by the bus agent*". Claim 48 is believed to be allowable because Gates does not discuss a means for allowing determination of an incorrect response to a sequence by a bus agent. Rather Gates discusses forcing an error response to a single instruction with an inverted parity bit. Claim 49 depends from claim 48 and is believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 50 and Dependent Claims

Claim 50 recites, "*An integrated circuit designed by defining a **legal** sequence of multiple phase bus transactions, asserting signals corresponding to the sequence of bus transactions on a bus, **capturing a response of an integrated circuit to the sequence of bus transactions, analyzing the response to detect a bug associated with an incorrect response to the legal sequence**, and correcting the bug*".

Claim 50 is believed to be allowable for at least the reason that Gates does not teach or suggest **capturing a response to a sequence of multiple phase bus transactions**. Rather, as discussed above Gates discusses forcing an error response by using a single command to invert a parity bit. Claims 51-54 depend from claim 50 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

35 U.S.C. §103(a) Rejection - Gates

The Examiner has rejected claims 3, 7 and 8 under 35 U.S.C. §103(a) as being unpatentable over Gates. These claims are believed to be allowable for the reasons discussed above.

Conclusion

Applicant respectfully submits that the rejections have been overcome by the amendments and remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed. The Examiner is requested to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: SEPT. 5, 2002 Brent E. Vecchia

Brent E. Vecchia
Reg. No. 48,011

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Claims:

Claim 1 remains unchanged.

Claims 3-14 remain unchanged.

Claims 16-19 remain unchanged.

Claims 21-24 remain unchanged.

Claims 31-54 remain unchanged.